

REMARKS

Claims 1-20 are pending in the present application.

Claims 1-8 and Claims 12-18 have been rejected.

Claims 9-11, Claim 19 and Claim 20 have been objected to.

Claims 1-20 remain in the case.

Reconsideration of Claims 1-20 is respectfully requested.

Amendments to the Specification

Paragraph [0155] of U. S. Patent Application Publication No. 2002 / 0097564 A1 was amended to correct a typographical error. No new matter was added to the specification as a result of the amendment.

Amendments to the Drawings

FIGURES 1, 3, 13 and 14 of U. S. Patent Application Publication No. 2002 / 0097564 A1 were amended to conform the figures to the text of the specification. No new matter was added to the drawings as a result of the amendments.

Objections to the Specification

On Page 2 of the January 9, 2004 Office Action, the Examiner stated that the title of the invention is not descriptive. The Examiner stated that a new title is required that is clearly indicative of the invention to which the claims are directed. In response Applicants respectfully traverse this assertion of the Examiner and respectfully submit that the title is descriptive. Applicants have not amended the title in view of Applicants' comments concerning the prior art and concerning rejections of the claims of the patent application.

Allowable Subject Matter

On Page 7 of the January 9, 2004 Office Action, the Examiner stated that Claims 9-11 and Claims 19-20 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants agree that Claims 9-11 and Claims 19-20 contain allowable subject matter. Applicants have not amended the claims in view of Applicants' comments concerning the prior art and concerning the rejections of the base claims of Claims 9-11 and Claims 19-20.

35 U.S.C. § 103(a) Obviousness

On Pages 2-5 of the January 9, 2004 Office Action, the Examiner rejected Claims 1-4, Claims 12-14 and Claim 18 under 35 U.S.C. § 103 (a) as being unpatentable over United States Patent No. 5,371,743 to *DeYesso et al.* (hereafter “*DeYesso*”) in view of United States Patent No. 6,253,267 to *Kim et al.* (hereafter “*Kim*”). On Pages 5-7 of the January 9, 2004 Office Action, the Examiner rejected Claims 5-8 and Claims 15-17 under 35 U.S.C. § 103 (a) as being unpatentable over *DeYesso* and *Kim* in view of United States Patent No. 6,363,437 to *Ptasinski et al.* (hereafter “*Ptasinski*”).

Applicants respectfully traverse the Examiner’s rejection of Claims 1-4, Claims 12-14 and Claim 18 as being obvious over *DeYesso* in view of *Kim*. Applicants respectfully request the Examiner to withdraw the rejection of Claims 1-4, Claims 12-14 and Claim 18 in view of Applicants’ remarks concerning the *DeYesso* reference and the *Kim* reference.

Applicants respectfully traverse the Examiner’s rejection of Claims 5-8 and Claims 15-17 as being obvious over *DeYesso* and *Kim* in view of *Ptasinski*. Applicants respectfully request the Examiner to withdraw the rejection of Claims 5-8 and Claims 15-17 in view of Applicants’ remarks concerning the *DeYesso* reference and the *Kim* reference and the *Ptasinski* reference.

During *ex parte* examinations of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to

deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of non-obviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 USPQ 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not be based on an applicant's disclosure. MPEP § 2142.

Applicants respectfully submit that the Patent Office has not established a *prima facie* case of obviousness with respect to the Applicants' invention.

Applicants direct the Examiner's attention to unique and novel elements of Claim 1 of the present invention:

1. (Original) For use in association with a backplane of an item of electronic equipment wherein said backplane comprises a common control bus that can access a first number of device locations, an apparatus capable of allowing said common control bus to access more than said first number of device locations, said apparatus comprising:

a complex programmable logic device on a circuit board card within said backplane, wherein said complex programmable logic device is coupled to said common control bus, and wherein said complex programmable logic device is capable of coupling each one of a plurality of device locations on said circuit board card to said common control bus. (Emphasis added).

The present invention as claimed in Claim 1 comprises an apparatus that is capable of allowing a common control bus to access more than a first number of device locations that are ordinarily accessible by a common control bus. The present invention provides a complex programmable logic device on a circuit board card that is coupled to the control bus wherein the complex programmable logic device is capable of coupling each one of a plurality of device locations on the circuit board card to the common control bus. Applicants respectfully submit that this feature is not disclosed, suggested or even hinted at in the prior art cited by the Examiner.

The Examiner stated "In regard to claims 1, 12 DeYesso et al. disclose the use in association with a backplane of the item of electronic equipment wherein the backplane comprising

a common control bus 15 that can access a first number of device locations, an apparatus capable of allowing the common control bus to access more than one first number of device locations (see figure 1, col. 3, line 17 through col. 4, line 37).” (January 9, 2004 Office Action, Page 2, Line 20 to Page 3, Line 3).

Applicants respectfully traverse this assertion of the Examiner. The *DeYesso* reference discloses an array 10 of a plurality of peripheral drive modules 11 such as data storage disks. In the example shown in FIGURE 1 of *DeYesso* a common power control bus 15 couples thirty (30) of the modules 11. The modules 11 are numbered from zero (0) to twenty-nine (29). Therefore the number thirty (30) is the first number of device locations in *DeYesso*. There is nothing in *DeYesso* that describes an apparatus that is capable of allowing the common power control bus 15 to access more than the first number (thirty) of device locations. The concept of providing an apparatus to enable a control bus to access more than a first number of device locations is completely absent from the *DeYesso* reference.

There is no plurality of devices on a circuit board card in the *DeYesso* device that is analogous to the plurality of devices on a circuit board card as in the Applicants’ invention. Each module 11 of *DeYesso* comprises a power/control circuit unit 11B. Each of the plurality of power/control circuit units 11B is connected to an external single I/O control processor 14 by means of an I/O connector 25. There is no apparatus in *DeYesso* for accessing additional device locations on a circuit board card.

The Examiner then stated that “But DeYesso et al. do not disclose the an apparatus comprising a complex programmable logic device (i.e. PLD) on the circuit board within the backplane, wherein the complex programmable logic device is coupled to the common control bus, and wherein the complex programmable logic device is capable of coupling each one of the plurality of device locations on the circuit board card to the common control bus.” (January 9, 2004 Office Action, Page 3, Lines 3-8). Applicants agree that *DeYesso* does not disclose a complex programmable logic device on a circuit board that is capable of coupling each one of a plurality of device locations on the circuit board card to a common control bus.

The Examiner then went on to state that “However, Kim et al. disclose programmable logic device (i.e. PLD) on the circuit board within the backplane, wherein the programmable logic device is coupled to the common control bus, and wherein the complex programmable logic device is capable of coupling each one of the plurality of device locations on the circuit board card to the common control bus (see col. 3, lines 7-49).” (January 9, 2004 Office Action, Page 3, Lines 8-13).

Applicants respectfully traverse this assertion of the Examiner. *Kim* discloses a hot-plug controller for a Peripheral Components Interconnect (PCI) bus that comprises a single integrated circuit chip. *Kim* discloses three embodiments: a single chip FPGA or ASIC circuit 50, a Hybride multi-chip circuit 70, and a daughter card 80. For example, circuit 50 comprises a system interface unit 10, a register unit 20, a power control unit 40, and a bus isolation unit 30. It is clear that bus isolation unit 30 of circuit 50 reads a control signal from the register unit 20 and, in response to

the control signal, either couples the PCI bus to or decouples the PCI bus from a single PCI slot. (*Kim*, Column 2, Lines 45-47). The *Kim* circuitry does not, however, couple each one of a plurality of device locations on a circuit board card to a common control bus. The *Kim* device controls the coupling of one PCI slot to a PCI bus. There is no teaching, suggestion or hint concerning the Applicants' concept of enabling a control bus to access more than a first number of device locations in a circuit board card. Therefore, it is clearly seen that the *Kim* reference is not capable of remedying the deficiencies of the *DeYesso* device.

The Examiner stated that "Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined the teachings of Kim et al. within the system of DeYesso et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip." (January 9, 2004 Office Action, Page 3, Lines 13-17). Applicants respectfully traverse this conclusion of the Examiner.

Under the applicable patent law, there must be some teaching, suggestion or motivation to combine the *DeYesso* reference and the *Kim* reference. "When a rejection depends on a combination of prior art references, there must be some teaching, or motivation to combine the references." *In re Rouffet*, 149 F.3d 1350, 1355-56, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998). "It is insufficient to establish obviousness that the separate elements of an invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the references." *Arkie Lures, Inc. v. Gene Larew Tackle, Inc.*, 119 F.3d 953, 957, 43 USPQ2d 1294, 1297 (Fed. Cir. 1997).

Applicants respectfully submit that there exists no teaching, suggestion or motivation in the prior art to combine the teachings of the *DeYesso* reference and the teachings of the *Kim* reference.

The Examiner suggested that a motivation to combine the references would be a desire to “reduce costs” and “increase reliability.” (January 9, 2004 Office Action, Page 3, Lines 15-17). Applicants respectfully submit that a general desire to “reduce cost” and “improve reliability” is too vague and general to serve as a legally sufficient motivation to combine references. There is nothing in a general desire to “reduce costs” that suggests combining the two references. The desire to reduce costs always exists for every technology and for every type of device. Similarly, there is nothing in a general desire to “improve reliability” that suggests combining the two references. The desire to improve reliability always exists for every technology and for every type of device. “Reducing costs” and “improving reliability” are not specific with respect to the two references but are applicable to every device in existence. In short, the motivation suggested by the Examiner to combine the references is simply too vague and general to be a legally sufficient motivation to combine the two references.

When two references are combined the combination of the references must teach or suggest all the claim limitations. In the present case, even if the *DeYesso* reference were combined with the *Kim* reference, the combination of the *DeYesso* reference and the *Kim* reference would not teach, suggest or even hint at the Applicants’ invention. This is because, as previously described, neither the *DeYesso* reference nor the *Kim* reference teaches, suggests, or even hints at the

Applicants' concept of enabling a control bus to access more than a first number of device locations in a circuit board card. Applicants respectfully submit that the rejection of Claim 1 under 35 U.S.C. §103(a) combining the *DeYesso* reference and the *Kim* reference should be withdrawn.

Claims 2-11 depend directly or indirectly from Claim 1. Claims 2-11 each contain the unique and novel elements of Claim 1. Therefore, Claims 2-11 each contain patentable subject matter. The Applicants respectfully submit that the rejections of Claims 1-4 under 35 U.S.C. §103(a) combining the *DeYesso* reference and the *Kim* reference should be withdrawn.

The Examiner also rejected Claims 12-14 and Claim 18 as being unpatentable as being obvious over *DeYesso* in view of *Kim*. Applicants respectfully traverse the Examiner's rejection of Claims 12-14 and Claim 18 as being obvious over *DeYesso* in view of *Kim*. Applicants hereby reiterate and incorporate by reference Applicants' previous comments concerning the *DeYesso* reference and the *Kim* reference. Applicants respectfully request the Examiner to withdraw the rejection of Claims 12-14 and Claim 18 in view of Applicants' remarks concerning the *DeYesso* reference and the *Kim* reference.

The Examiner also rejected Claims 5-8 and Claims 15-17 under 35 U.S.C. § 103(a) as being unpatentable over *DeYesso* in view of *Kim* and further in view of *Ptasinski*. Applicants respectfully traverse the Examiner's rejection of Claims 5-8 and Claims 15-17 as being obvious over *DeYesso* in view of *Kim* and in view of *Ptasinski*. Applicants hereby reiterate and

incorporate by reference Applicants' previous comments concerning the *DeYesso* reference and the *Kim* reference.

The Examiner stated that "In regard to claim 5, DeYesso et al. And Kim et al. teach the claimed subject matter as discussed above except the teaching of a card processor (i.e. controller) on the circuit board card within the back plane, the card processor coupled to the common control bus (see figure 7A, col. 3, lines 47-62)." (January 9, 2004 Office Action, Page 5, Lines 17-20). Applicants respectfully traverse this statement of the Examiner for the reasons that have previously been set forth.

The Examiner then stated that "Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined the teachings of Ptasinsky et al. within the system of DeYesso et al. and Kim et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip." (January 9, 2004 Office Action, Page 5, Lines 20-24). Applicants respectfully traverse this statement of the Examiner for the reasons that have previously been set forth.

Applicants respectfully submit that there exists no teaching, suggestion or motivation in the prior art to combine the teachings of the *DeYesso* reference and the teachings of the *Kim* reference and the teachings of the *Ptasinsky* reference. The Examiner suggested that a motivation to combine the references would be a desire to "reduce costs" and "increase reliability." (January 9, 2004 Office Action, Page 5, Lines 23-24). For the reasons previously set forth,

Applicants respectfully submit that the suggested motivation is too vague and general to serve as a legally sufficient basis for combining the references.

When two references are combined the combination of the references must teach or suggest all the claim limitations. In the present case, even if the *DeYesso* reference were combined with the *Kim* reference and with the *Ptasinski* reference, the combination of the *DeYesso* reference and the *Kim* reference and the *Ptasinski* reference would not teach, suggest or even hint at the Applicants' invention. This is because, as previously described, neither the *DeYesso* reference nor the *Kim* reference nor the *Ptasinski* reference teaches, suggests, or even hints at the Applicants' concept of enabling a control bus to access more than a first number of device locations in a circuit board card. Applicants respectfully submit that the rejection of Claim 5 under 35 U.S.C. §103(a) combining the *DeYesso* reference and the *Kim* reference and the *Ptasinski* reference should be withdrawn.

Claims 6-8 depend directly or indirectly from Claim 5. Claims 6-8 each contain the unique and novel elements of Claim 5. Therefore, Claims 6-8 each contain patentable subject matter. Applicants respectfully submit that the rejections of Claims 5-8 under 35 U.S.C. §103(a) combining the *DeYesso* reference and the *Kim* reference and the *Ptasinski* reference should be withdrawn.

The Examiner also rejected Claims 15-17 as being unpatentable as being obvious over *DeYesso* in view of *Kim* and in view of *Ptasinski*. Applicants respectfully traverse the Examiner's rejection of Claims 15-17 as being obvious over *DeYesso* in view of *Kim* and in view of *Ptasinski*.

Applicants hereby reiterate and incorporate by reference Applicants' previous comments concerning the *DeYesso* reference and the *Kim* reference and the *Ptasinski* reference. Applicants respectfully request the Examiner to withdraw the rejection of Claims 15-17 in view of Applicants' remarks concerning the *DeYesso* reference and the *Kim* reference and the *Ptasinski* reference.

Applicants respectfully submit that Claims 1-20 are all patentable over the *DeYesso* reference and the *Kim* reference and the *Ptasinski* reference whether taken individually or in combination. The Applicants respectfully request that the rejection of Claims 1-8 and Claims 12-18 be withdrawn and that Claims 1-20 be passed to issue.

Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Applicants reserve the right to submit further arguments in support of their above stated position as well as the right to introduce relevant secondary considerations including long-felt but unresolved needs in the industry, failed attempts by others to invent the invention, and the like, should that become necessary.

SUMMARY

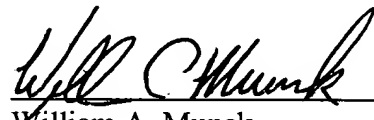
For the reasons given above, Applicants respectfully request reconsideration and allowance of pending claims and that this Application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this Application, Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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